International Journal of GEOMATE, March, 2019 Vol.16, Issue 55, pp. 20 - 27
ISSN: 2186-2982 (P), 2186-2990 (O), Japan, DOI: https://doi.org/10.21660/2019.55.4510
Special Issue on Science, Engineering & Environment

SPICE MODEL OF DRAIN INDUCED BARRIER LOWERING IN SYMMETRIC JUNCTIONLESS DOUBLE GATE MOSFET

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*Corresponding Author, Received: 20 Oct. 2018, Revised: 30 Nov. 2018, Accepted: 25 Dec. 2018

ABSTRACT: A SPICE model of Drain Induced Barrier Lowering (DIBL) has been proposed for a symmetric junctionless double gate (JLDG) MOSFET. For this purpose, the potential distribution in the channel is obtained using the Poisson equation, and the threshold voltage is determined by the third derivative (TD) method. The SPICE model of DIBL should be expressed as a function of silicon thickness t_{si} as well as channel length L_g, oxide thickness t_{ox}, and SPICE parameter η such as $\sigma_D=A\eta L_g^{-3} t_{si}^2 t_{ox}$ due to the effect of silicon thickness on carrier transport in a nanostructure JLDG MOSFET, even though it is only defined by channel length and oxide thickness in SPICE model of conventional MOSFET. As a result, it is found that the proportional constant A is 22.0 and the static feedback coefficient η is reasonably between 0.2 and 0.9. The DIBLs obtained by using the threshold voltage model published in other papers show a good agreement with those of this model regardless of the channel length at 20 nm or more, but the DIBLs of the other models are different at the sub-20 nm channel lengths from one another due to approximations of each other. Also we show that the DIBL for JLDG MOSFET is smaller than junction-based double gate MOSFET.

Keywords: Junctionless double gate, Threshold voltage, DIBL, Static feedback coefficient

1. INTRODUCTION

The conventional MOSFET structure is no longer usable due to the short channel effect in the structure below 20 nm. In particular, it is necessary to improve the subthreshold swing degradation, threshold voltage roll-off, drain induced barrier lowering (DIBL), and the ON/OFF current ratio due to the increase of the power consumption by the increase of the parasitic current, and it is required to improve the control ability of the carriers in the channel by the gate voltage. In addition, the variation of the doping concentration between the source/drain region and the channel shows the limit of junction based double gate (JBDG) MOSFET process as well as the conventional MOSFET while the channel length is decreased [1]. To solve this problem, the transistor structure of a junctionless double gate (JLDG) MOSFET is developed. The JLDG MOSFET has advantages of simplifying the process because it has no junctions between source/drain and channel, and it can use the existing MOSFET process as well as reducing the process cost. Therefore, transport model and process development for a JLDG MOSFET as well as junctionless structure FET such as junctionless cylindrical surrounding gate (JLCSG) MOSFET are under study [2]-[4]. Especially, it is necessary to develop a model for SPICE simulation because it has reached the stage of analyzing characteristics in circuit configuration using a JLDG MOSFET [5]. Therefore, in this paper, we propose the SPICE-used model of DIBL σ_D, induced by deviation of threshold voltage due to the change of drain voltages in JLDG MOSFET, known as the short channel effect. The threshold voltage will be derived from the transfer characteristics between the drain current and the gate voltage by the third derivative (TD) method that has already been verified [6].

The σ_D for JBDG MOSFET to operate in inversion mode has been proposed [7]. In the case of JLDG MOSFETs to operate in accumulation mode, the channel shows a fully depleted state in the subthreshold voltage, and is partially depleted at the threshold voltage, indicating the on-state characteristic as the current flows into the partially formed neutral region [8]. When the gate voltage further increases to reach a flat voltage, the entire channel becomes a neutral state and enters the accumulation state. In the conventional MOSFET, the current amount is determined by the amount of charge formed in the inversion layer. The inversion layer thickness has more influence on the current amount than the silicon thickness in the case of the conventional MOSFET, but the amount of current for the JLDG MOSFET will be determined, depending on the oxide film thickness and silicon thickness as well as channel length. Therefore, in this paper, the σ_D will be expressed mathematically after observing the change of DIBL according to channel length, silicon thickness, and oxide thickness. The model will be set so that the static feedback coefficient η, which is a SPICE parameter of σ_D, has a reasonable value.

Raksharam et al. described the change in the threshold voltage for a JLDG MOSFET with a

channel length of 22 nm as an analytical threshold voltage model [9]. Jiang et al. defined the threshold voltage using the potential distribution of the series form and expressed analytically the change of threshold voltage due to drain voltage [10]. In addition, Lin et al. obtained the potential distribution by solving the one-dimensional Poisson equation and the two-dimensional Laplace equation, and calculated the threshold voltages for JLDG MOSFETs with channel lengths of 20 nm or more [11]. We will verify the validity of the proposed model by comparing the DIBL values derived from the threshold voltage model obtained from other papers with those procured from the model presented in this paper.

In Section 2, we will explain the DIBL derivation process using the analytical potential distribution and current-voltage characteristics of JLDG MOSFETs. In Section 3, we will present the SPICE-used model by analyzing the obtained DIBL according to the channel structure. Conclusions are given in Section 4.

2. POTENTIAL DISTRIBUTION AND DIBL OF JLDG MOSFET

2.1 Potential Distribution of JLDG MOSFET

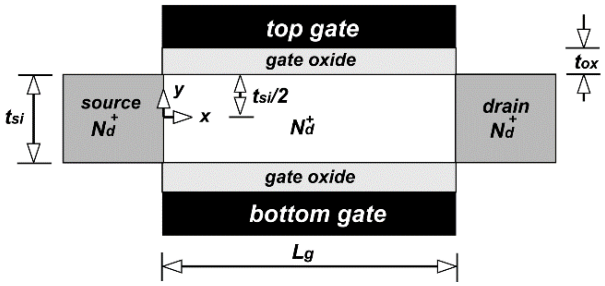

Fig. 1 Schematic cross sectional diagram of Junctionless Double Gate (JLDG) MOSFET. The doping concentration of source/drain and channel is nearly equal.

Figure 1 shows the cross sectional view of JLDG MOSFET. As shown in Fig. 1, the JLDG MOSFET is a junctionless structure with the same doping type and concentration for source/drain and channel. If channel doping is p-type or undoped in Fig. 1, we can calculate transport characteristics for junction based double gate MOSFET. In this study, $N_d=10^{19}/cm^3$ is used. Most of the carriers in the symmetrical structure will be transmitted through the center of the channel in the case of JLDG MOSFET to operate in accumulation mode, and the potential distribution is obtained using the following Poisson equation and the boundary conditions when the channel length changes from 10 nm to 50 nm, the silicon thickness from 5 nm to 10 nm, and the oxide thickness from 1 nm to 4 nm.

$$\frac{\partial^2\phi}{\partial x^2}+\frac{\partial^2\phi}{\partial y^2}=-\frac{qN_d}{\varepsilon_{si}} \tag{1}$$

$$\phi(0,y)=V_{ref}$$
$$\phi(L_g,y)=V_{ref}+V_{ds}$$
$$\left.\frac{\partial\phi}{\partial y}\right|_{y=0}=0$$
$$\left.\frac{\partial\phi}{\partial y}\right|_{y=\frac{t_{si}}{2}}=\frac{\varepsilon_{ox}}{\varepsilon_{si}t_{ox}}\left[V_{gs}+V_{FB}-\phi(x,\frac{t_{si}}{2})\right]$$

where V_{ref} is the reference potential, V_{ds} the drain voltage, V_{gs} the gate voltage, V_{FB} the flat band voltage, and ε_{si} and ε_{ox} are the dielectric constants of silicon and oxide film, respectively.

In the case of JLDG MOSFET, as shown in Jiang et al.'s method, the potential distribution can be obtained as follows [10].

$$\phi(x,y)=V_{ref}+\frac{V_{ds}}{L_g}x+\sqrt{\frac{2}{L_g}}\sum_{n=1}^{\infty}\left[2C_n\cosh(k_ny)-\frac{f_n}{k_n^2}\right]\sin\left(\frac{n\pi}{L_g}x\right) \tag{2}$$

$$C_n=\frac{1}{2\alpha_n}\left[\frac{f_n}{k_n^2}+\sqrt{\frac{2}{L_g}}\frac{(-1)^{-n}}{k_n}(V_{ds}+V_{FB}-V_{gs})-\sqrt{\frac{2}{L_g}}\frac{1}{k_n}(V_{FB}-V_{gs})\right]$$

$$f_n=-\frac{qN_d}{\varepsilon_{si}k_n}\sqrt{\frac{2}{L_g}}[1-(-1)^n],\ k_n=\frac{n\pi}{L_g}$$

$$\alpha_n=t_{ox}\frac{\varepsilon_{si}}{\varepsilon_{ox}}k_n\sinh\left(\frac{t_{si}k_n}{2}\right)+\cosh\left(\frac{t_{si}k_n}{2}\right)$$

In this study, we used the results calculated up to n= 30 because n=30 is larger enough for a good approximation [12].

2.2 DIBL of JLDG MOSFET

The potential distributions derived from Eq. (2) are shown in Fig. 2 for channel lengths of 20 nm and 40 nm. The schematic diagram of σ_D is also shown as plotting the potential distribution for drain voltages of 0.05 V and 0.55 V as shown in Fig. 2. It can be found

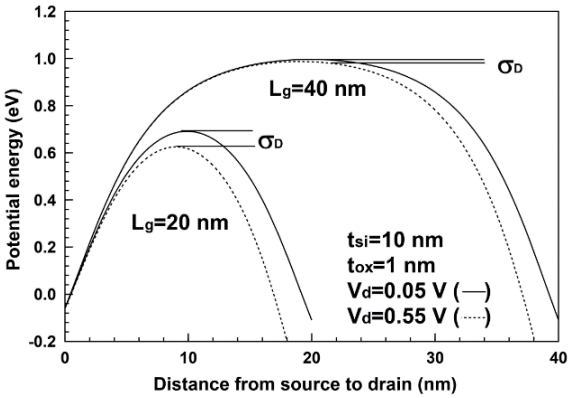

Fig. 2 Potential distributions for the changes of drain voltage and channel length.

that the potential distribution of source side is reduced with increasing of the drain voltage. As shown in Fig. 2, the degree of reduction for the maximum potential increases according to the decrease of the channel length due to short channel effects. We know the threshold voltage is changed according to the deviation of potential distribution because the thermionic emission current from source to drain depends on the potential distribution. The silicon thickness and oxide thickness as well as channel length will affect the potential distribution. This changes carrier transport from source to drain, so drain current is changed. As a results, we have to know the potential dependent drain current to obtain the threshold voltage.

The relationship between the drain current and the gate voltage is derived from the diffusion-drift current equation of Eq. (3) to obtain the threshold voltage.

$$I_d = \frac{qn_i\mu_n WkT\left\{1-\exp\left(\frac{-qV_{ds}}{kT}\right)\right\}}{\int_0^{L_g}\frac{1}{\int_{-\frac{t_{si}}{2}}^{\frac{t_{si}}{2}}\exp\left(\frac{-q\phi(x,y)}{kT}\right)dy}dx} \quad (3)$$

where W is the channel width, n_i is the intrinsic semiconductor concentration of silicon, μ_n is the mobility, k is the Boltzmann constant and T is the absolute temperature. Since the validity of Eq. (3) is described in the previous paper [13], the relationship between drain current and gate voltage obtained using Eq. (3) is used to obtain the threshold voltages. Figure 3(a) shows the relationship between drain current and gate voltage obtained in this study. We used the TD method proposed by Wong et al. [6] to extract the threshold voltage. As shown in Fig. 3(b), the threshold voltage is extracted as the minimum of the third-order differential coefficient obtained by using the current-voltage relationship in Fig. 3(a) because the TD method can be used efficiently in determining the threshold voltage including the physical meaning.

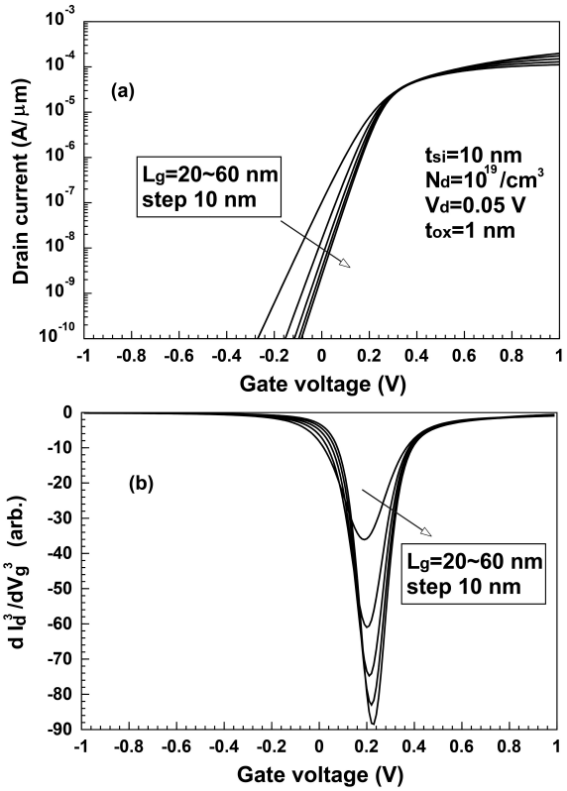

Fig. 3 (a) Transfer characteristics for drain current vs. gate voltage with channel length as a parameter, and (b) the threshold voltage extraction method by third derivatives for transfer characteristics of (a).

As shown in Fig. 3(b), the gate voltage corresponding to the inflection point of the curve is defined as the threshold voltage, and the DIBL is obtained using the following Eq. (4).

$$\sigma_D = \frac{\left[V_{th}(V_{ds}=0.05\,V)-V_{th}(V_{ds}=0.55\,V)\right]}{0.5} \quad (4)$$

In general, the DIBL is varied according to the channel size and oxide thickness, and DIBL model σ_D in SPICE is expressed using these variables and the static feedback coefficient η as a parameter. In the conventional MOSFET, the static feedback coefficient η is generally 0.7 [14]. In this paper, we propose SPICE model of DIBL which depends on channel size and oxide thickness with reasonable static feedback coefficient η for the JLDG MOSFET. In the nanostructure JLDG MOSFET, unlike the conventional MOSFET, the size of the channel must be involved in obtaining DIBLs because the entire channel affects current flow when JLDG MOSFET changes from a fully depleted state to a partially depleted state. That is, not only the channel length but also the silicon thickness will affect the carrier transmission. It is known that the σ_D is proportional to L_g^{-3} for the channel length in the conventional MOSFET [14]. In addition, the σ_D is proportional to

the square of silicon thickness for a nanostructure junction-based double gate MOSFET [7]. Therefore, in this paper we will derive the σ_D of JLDG MOSFET including all of the above mentioned variables.

3. SPICE MODEL OF DIBL FOR JLDG MOSFET

3.1 Extraction of Static Feedback Coefficient

In this paper, we use Eq. (4) to find the DIBL from threshold voltage at the drain voltage of 0.05 V and 0.55 V, and present the SPICE-used DIBL model by observing the change of DIBL, with respect to channel length, silicon thickness and oxide thickness.

Figures 4(a), 4(b), and 4(c) show the variation of DIBLs with respect to channel length, silicon thickness, and oxide thickness, respectively. As shown in Fig. 4(a), the relation of $\sigma_D \propto L_g^{-3}$ is indicated by a dotted line to observe whether DIBL is proportional to L_g^{-3}. Figures 4(a) and (b) use alogarithm-logarithm graphs. In these graph, it is easy to grasp the multiplier by using the slope of the straight line since the relationship appears as a straight line. As shown in Fig. 4(a), the σ_D for the channel length is proportional to the power of -3 as in the conventional MOSFET. Figure 4(b) shows the change in DIBL with respect to the silicon thickness, with the relation of $\sigma_D \propto t_{si}^2$ denoted as a dotted line, and the σ_D shows good agreement with the proportional relation to the power of 2 for silicon thickness. As shown in Fig. 4(b), the inclination is the same when the channel length is 10 nm and 20 nm. Finally, in order to observe the relationship between oxide thickness and DIBL, the relationship between DIBL and oxide thickness is shown in Fig. 4(c) when the silicon thickness is 5 nm and 7 nm with the channel length as a parameter. Note that the linear scale for x and y axis is used in Fig. 4(c), unlike Figs. 4(a) and (b). As shown in Fig. 4(c), the relations between DIBL and oxide film thickness are linear regardless of channel length and silicon thickness although the slope is different. The σ_D will be inversely proportional to the gate oxide capacitance since it is linear to the oxide thickness. That is, the influence of the gate voltage on the carrier transmission in the channel will be further blocked when gate oxide capacitance increases; as a result, the carrier transmission control ability of the gate voltage will be weakened. The threshold voltage will be less affected and the DIBL will also decrease as the oxide film thickness decreases. Therefore, it is reasonable to assume that the σ_D representing DIBL in Eq. (4) is linearly proportional to t_{ox}. As a result, the σ_D can be expressed as a function of channel length, silicon thickness, and oxide thickness like the following Eq. (5).

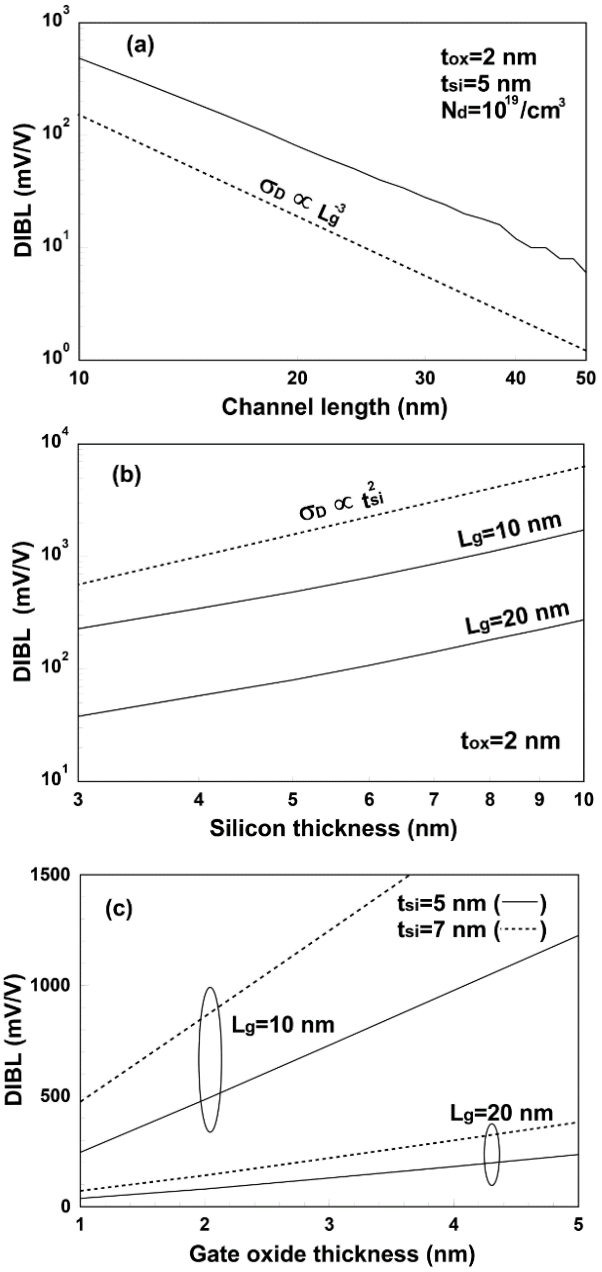

Fig. 4 (a) DIBLs for channel length of JLDG MOSFET. Dotted line denotes proportional line for power of -3 for channel length, (b) DIBLs for silicon thickness of JLDG MOSFET with channel length as a parameter. The dotted line denotes proportional line for power of 2 for silicon thickness, and (c) DIBLs for gate oxide thickness of JLDG MOSFET with channel length as a parameter for silicon thickness of 5 and 7 nm. We know DIBLs are proportional for power of 1 for gate oxide thickness.

$$\sigma_D = A\eta L_g^{-3} t_{si}^2 t_{ox} \quad . \tag{5}$$

In the case of the JLDG MOSFET of Eq. (5), the SPICE-used DIBL model, which can be expressed by

only the channel size and the oxide thickness, is derived by setting the A value to have the static feedback coefficient η of between 0 and 1 that is SPICE parameter of σ_D. First, the value of $A\eta$ in Eq. (5) is obtained in the range of channel length between 10 nm and 50 nm, silicon thickness between 5 nm and 10 nm, and gate oxide thickness between 1 nm and 4 nm, and the maximum value of $A\eta$ is set as A to sustain the static feedback coefficient η between 0 and 1. The value of A thus obtained is 22.0. Therefore, the SPICE-used DIBL model of the JLDG MOSFET can be obtained as follows.

$$\sigma_D = 22.0\eta L_g^{-3} t_{si}^2 t_{ox} \tag{6}$$

Figure 5 shows the static feedback coefficient η obtained using Eq. (6) from the range of the channel size and the oxide thickness as mentioned in the previous paragraph. As can be seen in Fig. 5, the values of η is ranged from 0.2 to 0.9. As the channel length increases, the variation rate of η increases. Especially, the variation of the static feedback coefficient η increases as the oxide thickness and silicon thickness increases. Note that it is small enough that the η varies between 0.4 and 0.8 as known in the results in Fig. 5 (a) with oxide film thicknesses down to 1 nm. From the above results, it can be concluded that Eq. (6) is a SPICE-used DIBL model which can fully express the DIBL phenomenon of JLDG MOSFET.

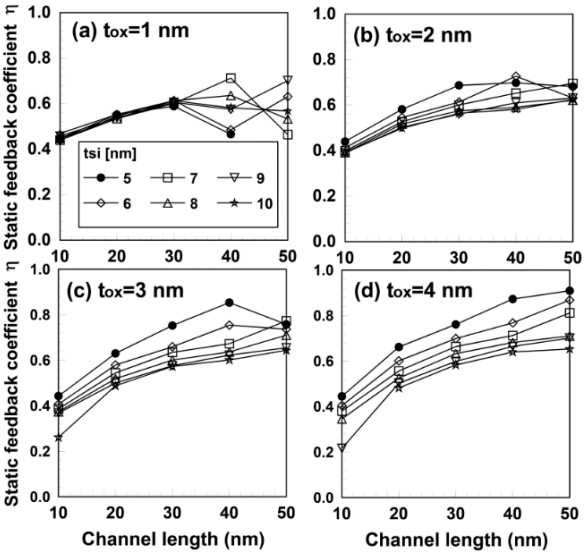

Fig. 5 Static feedback coefficients for JLDG MOSFET in the range of 10 nm ≤ L_g ≤50 nm, 5 nm ≤ t_{si} ≤10 nm and (a) t_{ox}=1 nm (b) t_{ox}=2 nm, (c) t_{ox}=3 nm, and (d) t_{ox}=4 nm.

3.2 Comparison of this model and other models

In order to verify the validity of Eq. (6) presented in this paper, the results of the comparison with the

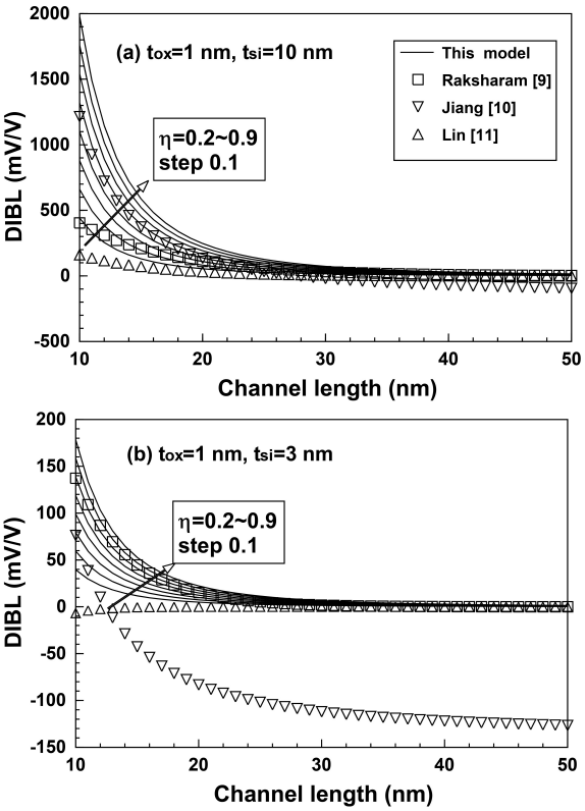

Fig. 6 Comparisons of this model with various models for DIBL of JLDG MOSFET in the range of 10 nm ≤ L_g ≤50 nm and (a) t_{ox}=1 nm, t_{si}=10 nm , and (b) t_{ox}=1 nm, t_{si}=3 nm.

DIBL values obtained using the threshold voltage model presented in other papers are shown in Fig. 6.

Figure 6 shows the DIBLs of this model with solid lines in the range of $0.2 \le \eta \le 0.9$. As shown in Fig. 6(a), the DIBLs of this model are good agreement with other DIBLs. Since the potential model used in this paper basically uses the model proposed by Jiang et al., it can be seen that the results are in good agreement with the results of Jiang's model in the range of $0.5 \le \eta \le 0.6$, in the case of Fig. 6(a) with the silicon thickness of 10 nm.

Compared with Lin's model, results of Lin's model show good agreement with those of other models only when the channel length is relatively long. Actually, Lin et al. calculated for the channel length over 20 nm and found that results agree well with other models in this range. However, there is a large difference from other models at a channel length of 20 nm or less because Lin's model only used n=1 and assumed $\sinh(x) \approx 0.5\exp(x)$ in Eq. (2). Even though Raksharam's model uses a different potential distribution model than the one proposed in this study, it is observed that their results are good agreement to other results when the silicon thickness and the oxide thickness are small as shown in Fig. 6(b). The potential distribution for Raksharam's model is the followings;

$$\phi(x,0) = (V_{gs} - V_{TH})\left(1 - \frac{\sinh\left(\frac{x}{\lambda}\right) + \sinh\left(\frac{L_g - x}{\lambda}\right)}{\sinh\left(\frac{L_g}{\lambda}\right)}\right) + V_{ds}\left[\frac{\sinh\left(\frac{x}{\lambda}\right)}{\sinh\left(\frac{L_g}{\lambda}\right)}\right] \quad (7)$$

$$\lambda = \sqrt{\frac{\varepsilon_{si} t_{si} t_{ox}}{2\beta\varepsilon_{ox}}}$$

where β is parameter, and V_{TH} is the threshold voltage. Unlike the other models, the Raksharam's model has parameter β for matching with this model. To compare with this model, we use β =0.8. As a result, the results of Raksharam's model agree well with this model. The results are well matched regardless of the model in the range of the channel length of 20 nm or more except Jiang's model, but note the differences of DIBL models are more significant in case that the channel length is 20 nm or less.

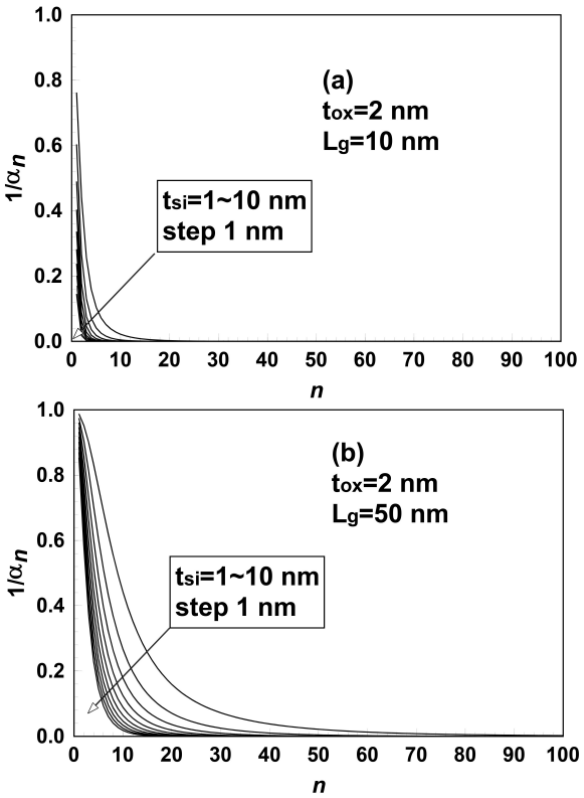

Fig. 7 Deviations of $1/\alpha_n$ for higher order terms in Jiang et. al.'s potential model in the range of (a) t_{ox}=2 nm, L_g=10 nm, and (b) t_{ox}=2 nm, L_g=50 nm.

The smaller the silicon thickness, the greater the difference between Jiang's model and this model. The reason for this is that Jiang et al. calculated the potential distribution using the series form and defined the threshold voltage model using only the first term. That is, the smaller the silicon thickness becomes, the larger the error between Jiang's model and this model is. It is clear that Jiang's model shows a big difference from other models as the channel length increases in Fig. 6(b) due to this reason. The deviation between this model and Jiang et al.'s model increases as the channel length increases as shown in Fig. 6(b).

To clarify this point, Fig. 7 shows the variation of $1/\alpha_n$ in Eq. (2) which is used to calculate the threshold voltage in the Jiang's model. As shown in Fig. 7, when n increases, the value of $1/\alpha_n$ sharply decreases, and the value of $1/\alpha_n$ decreases more sharply with increasing silicon thickness and smaller channel length. If the silicon thickness is small and the channel length is large, it can be seen that the approximation of n = 1 in Eq. (2) is not valid.

3.3 Comparison of JBDG and JLDG MOSFETs

The JLDG MOSFETs to operate in accumulation mode have better short channel effect than the JBDG MOSFET known as inversion mode device [15]. We compared the SPICE-used DIBL model of the previous paper [7] for JBDG MOSFET with this model for JLDG MOSFET. Table 1 shows the constant A and static feedback coefficient η for JBDG and JLDG MOSFET, and Fig. 8 shows the minimum and maximum values of the DIBLs according to channel length derived from the values of Table 1. As shown in Fig. 8, the DIBLs for JLDG MOSFETs is lower than those of JBDG MOSFETs. The maximum values of DIBLs for JBDG and JLDG MOSFET is nearly equal regardless of channel length. This is because the SPICE-used DIBL model presented, regardless of JBDG and JLDG MOSFET, sets the constant A and static feedback coefficient η to accommodate a sufficiently large DIBL value. However, the minimum values show the significant difference, especially in the range of short channel length. It can be seen that as the channel length is shortened, the JLDG MODFETs not only overcome the process limit to make PN junction such as JBDG MOSFET, but also improve the short channel effect like DIBL more than the JBDG MOSFETs.

Table 1. A and η for JBDG and JLDG MOSFETS

Type	A	η	Ref.
JBDG	11.36	$1 \le \eta \le 2$	[7]
JLDG	22.0	$0.2 \le \eta \le 0.9$	

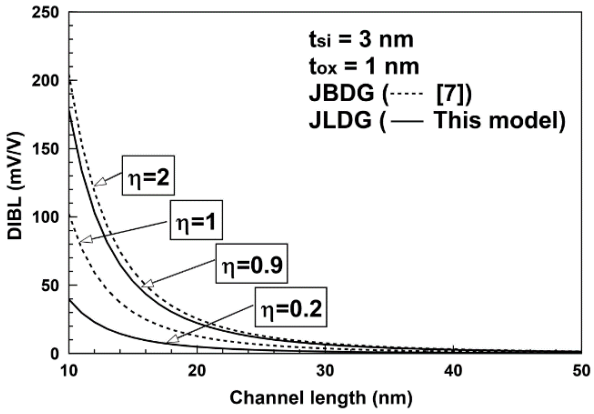

Fig. 8 Comparisons of the SPICE used DIBL model for JBDG MOSFET and JLDG MOSFET.

4. CONCLUSION

In this paper, a SPICE-used DIBL model for a JLDG MOSFET has been presented. Since the parameters of the SPICE-used DIBL model are static feedback coefficients, the model equations are constructed to represent the reasonable range in the SPICE simulation. For this purpose, the threshold voltage was derived by the TD method in the relation between drain current and gate voltage to obtain using the potential distribution of the series form derived from the Poisson equation. The validity of the DIBL obtained using this threshold voltage was verified by comparing it with other papers. As a result, it was found that the σ_D representing DIBL is proportional to the channel length by the power of -3, the silicon thickness by 2, and the oxide thickness by 1 where the proportional constant A is 22.0. In this case, the static feedback coefficient η, SPICE parameter, is found in the range of 10 nm $\leq L_g \leq$50 nm, 5 nm $\leq t_{si} \leq$10 nm, 1 nm $\leq t_{ox} \leq$4 nm**,** and is in the range of $0.2 \leq \eta \leq 0.9$. The variation of the static feedback coefficient η decreased with decrease in the oxide and silicon thickness. Especially, the static feedback coefficient η was nearly constant regardless of the silicon thickness when the oxide thickness was 1 nm and the channel length was below 30 nm. In comparison of JBDG and JLDG MOSFETs, it was found that JLDG structure had better DIBL value. These results will be useful for circuit simulation using JLDG MOSFET.

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